AD-A182 486 IN-SITU MOS GATE ENGINEERING IN A NOVEL RAPID THERMAL/PLASMA MULTIPROCESSING REACTOR(U) STANFORD UNIV CA CENTER FOR INTEGRATED SYSTEMS M M MOSLEHI ET AL. 1/1

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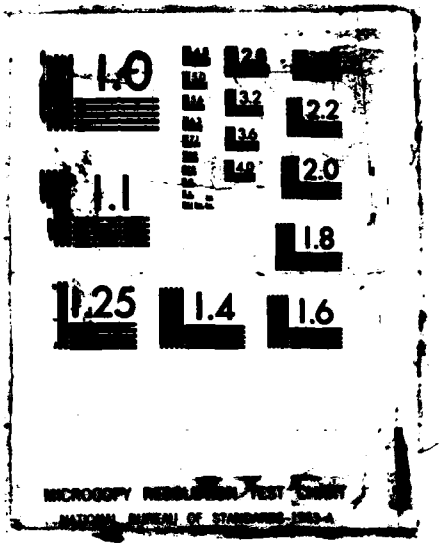
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SUBMITTED TO VLSI SYMP. 1987 (1)

IN-SITU MOS GATE ENGINEERING IN A NOVEL RAPID THERMAL/PLASMA MULTIPROCESSING REACTOR

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Low temperatures and short times are essential requirements of future VLSI processing and the use of plasma in conjunction with single-wafer lamp heating is a major step to realize this goal. *In-situ* multiprocessing reduces contamination and enhances yield. Reproducible growth of thin oxides in hot-wall furnaces is difficult due to long transient times and constant furnace temperatures. Since furnaces are not designed for single-wafer processing, no extensive *in-situ* real-time measurements can be performed. RTP of Si in O_2 and NH_3 ambients is an attractive technique for the growth of silicon nitride, silicon dioxide, nitrided oxides, oxidized nitrides, and application-specific insulators [1]. We have also demonstrated the feasibility of low-temperature nitridation of Si in nitrogen plasma generated by microwave discharge [2]. LPCVD of tungsten (W) has emerged as a viable technology for VLSI. The conventional hot-wall furnaces are not suitable for reproducible high-rate W deposition and nonselective formation of W on insulators.

Based on our experiences with microwave plasma nitridation and the rapid thermal dielectric growth and anneal processes, we have developed a novel cold-wall single-wafer rapid thermal/plasma multiprocessing reactor for *in-situ* growth and deposition of dielectrics, silicon, and metals (Fig. 1). This equipment is the result of an attempt to enhance equipment versatility, to improve process reproducibility and uniformity, to increase growth and deposition rates, and to achieve *in-situ* multiprocessing. The water-cooled stainless steel chamber provides various ports for gas injection, optical heating of the wafer, pump, and *in-situ* process monitoring. The wafer sits on low thermal mass pins facing the end cone of a discharge tube and is heated on the other side by tungsten-halogen lamps. The optical flux reaches the wafer through a water-cooled quartz window. The wafer temperature can be controlled in a range from room temperature to 1150 for seconds up to many minutes. Any combination of

Ar, N_2, O_2, NH_3, WF_6, WCl_6, H_2, SiH_4, and SF_4 can be injected into the chamber either through a quartz tube at the bottom of the chamber or through the side port nonplasma injectors. Remote plasma can be generated inside the tube by a microwave discharge cavity. The availability of plasma processing not only allows low-temperature dielectric growth but also has enabled us to develop several new processes for nonselective deposition of W and its compounds on insulating layers for MOS gate applications. This system configuration is very flexible for *in-situ* multiprocessing because it allows rapid cycling of ambient gases, temperature, and plasma with negligible cross-contamination. The details of this reactor are presented elsewhere [3].

The rapid thermal oxidation (RTO) process is a viable technique for growing thin . The MOS devices with rapidly grown were found to have larger charge-to-breakdown and lower electron trapping compared to furnace oxides. As an example, the charge-to-breakdown vs RTO temperature shown in Fig. 2 indicates a higher breakdown charge when the surface is free of native oxide prior to gate oxidation. This demonstrates the importance of *in-situ* preoxidation surface cleanliness because the chemical oxide simulates the oxide grown in a furnace when the wafers see uncontrolled ambient and temperature during loading and unloading. As compared to the devices with preoxidation removal of native oxide, the presence of a chemical oxide prior to RTO reduced Q_f and D_{it}, and their dependencies on the RTO temperature. Multicycle rapid thermal growth processes are suitable for dielectric engineering and *in-situ* formation of thin layered insulators with a variety of controllable oxygen and nitrogen compositional depth profiles by appropriate design of the temperature and gas cycles. In the rapid thermal nitridation (RTN) of , N-rich layers form at the surface and interface (Fig. 3(a)). RTN of slows down the generation rate of new surface states caused by high-field electrical stress (Fig. 3(b)). To demonstrate the multiprocessing capabilities of RTP, we have fabricated various NMOS transistors where RTP was employed for growth and annealing of gate oxides and nitrocides, activation and redistribution of dopant in source/drain and polysilicon gates, growth of polysilicon oxides, and forming gas anneals. Some results regarding electrical performance, hot-carrier degradation, and surface mobilities of IGFETs with rapidly grown gate insulators will be presented.

The main objective of our work was to develop reliable processes for *in-situ* fabrication of W-gate MOS devices which requires the growth of gate dielectric by RTO and RTN cycles followed by a nonselective W deposition process to form the gate electrode. W is quite attractive as an MOS gate material [4]; however, a reliable process for *in-situ* formation of W gate electrodes has not been developed. W-gate MOS VLSI can be realized if some of the major problems related to the poor adhesion of W to insulating layers, channeling of

implanted dopants through W gate, and lack of oxidation resistance are overcome. We have used two approaches to solve this problem: one by using a Si glue layer and the other by the use of RTP/microwave plasma technology.

H_2 reduction of WF_6 can not occur on insulators unless some layer of metal or Si is used for initial nucleation. In a series of experiments, W deposition by a conventional hot-wall LPCVD furnace on using amorphous Si as a glue layer was investigated. For 30 min of W deposition, the W films on oxidized wafers coated with 340 and 430 of LPCVD amorphous Si successfully passed the transparent tape adhesion test. An average sheet resistance of 0.9 Ω/□ for 1300 W films was obtained. W peeled off from wafers coated with 250 of amorphous Si after only 20 min of W deposition which indicated that the presence of some amorphous Si was needed for adequate adhesion. W-gate MOS capacitors were fabricated using this technique and Fig. 4 illustrates the typical C-V characteristics. The densities of midgap D_{it} were in the range of $(2.5\text{-}3.5)10^{10}$ $eV^{-1}cm^{-2}$. The insulator thickness estimated by the C-V method was consistently thicker (by as much as 30 to 55) than the oxide thickness measured before the amorphous Si deposition which is an indication of some remaining excess amorphous Si; however, this Si was completely consumed during subsequent thermal annealing.

As a result of the process limitations of the above technique a variety of selective and nonselective processes were investigated in this work using the novel reactor. Table 1 presents a summary list of the W deposition processes developed using our multiprocessing reactor. These techniques are grouped based on the plasma condition and the injection mode of various ambient gases. These depositions were studied extensively in a wide range of gas flows, pressure, and temperature. Several of these novel nonselective processes are reported for the first time in this work. When WF_6 or a mixture of WF_6+H_2 was injected through the nonplasma part, generation of H_2 plasma, Ar plasma, or Ar+H_2 plasma in the quartz tube promoted nonselective W deposition on insulating surfaces. Addition of Ar to H_2 enhances the plasma emission intensity and density of available atomic hydrogen. Another nonselective deposition technique developed in this work employed WF_6+Ar plasma along with nonplasma H_2. Under appropriate experimental conditions none of these nonselective deposition techniques caused W deposition on the chamber walls or inside the quartz tube. The mixture of NH_3+H_2 and WF_6 always resulted in nonselective deposition for both plasma and nonplasma types of processes. Moreover, the combination of N_2+H_2 plasma and WF_6 also resulted in nonselective metallic film deposition. The films deposited by any of the last three techniques in Table 1 (rows J,K,L) had higher resistivities compared to pure W and were expected to be W nitride compounds. W nitride may exhibit several properties such as oxidation resistance, diffusion barrier, and ion implant channeling stop. W nitride films could also be formed by

RTN of W layers. The films nitrided at the highest temperature (1000 or more) were not stable; however, the W films nitrided at lower temperatures (e.g. 825) were stable. According to the Auger depth profiles the films nitrided at 825 and above were W oxynitrides. *In-situ* adhesion to insulators was obtained for nonselective deposited W films thicker than 1 . In some instances, an initial W deposition cycle was followed by another type of deposition in order to obtain optimal adhesion and uniformity properties. All of the nonselective deposition techniques developed in this work are applicable to *in-situ* fabrication of metal gate MOS devices. Various *in-situ* MOS devices were successfully fabricated using these techniques and the results including studies of possible plasma damage will be presented.

Any combination of $WF_6/H_2/Ar$ without plasma discharge (rows A through E in Table 1) resulted in very selective W depositions on exposed Si areas. The selective depositions were performed in a wide range of gas flow rates, pressure, and temperature and selectivity was maintained for depositions well over 1 . Compared to a furnace, this single-wafer cold-wall reactor offers a much larger processing window for selective processes without loss of selectivity after long times at elevated temperatures as much as 450.

In conclusion, this novel rapid thermal/plasma multiprocessing technique has potential merits for *in-situ* fabrication of future MOS VLSI circuits. This work was supported by IBM, DARPA, and SRC.

[1] M. Moslehi *et al.*, ECS Proc. 86-4, 379 (1986).
[2] M. Moslehi *et al.*, J. Appl. Phys. 58, 2416 (1985).
[3] M. Moslehi *et al.*, MRS Symp. on RTP, (1987).
[5] N. Kobayashi *et al.*, VMIC Proc., 436 (1986).

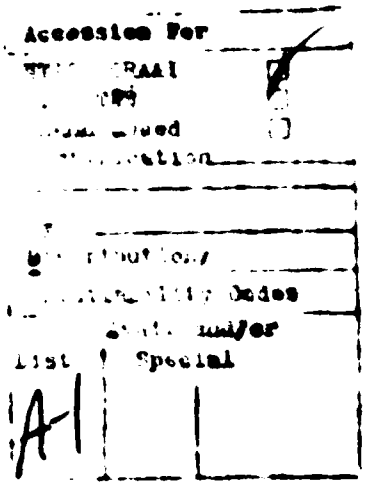

Table 1: Various types of plasma and nonplasma tungsten LPCVD experiments performed in this work.

Deposition Type	Gases through the Quartz Tube	Gases through the Side Ports	Microwave Power	Deposition Condition
A	None	WF_6+Ar	OFF	Selective
B	None	WF_6+H_2	OFF	Selective
C	Ar	WF_6+H_2	OFF	Selective
D	WF_6	WF_6+H_2	OFF	Selective
E	H_2	WF_6	OFF	Selective
F	H_2	WF_6	ON	Nonselective
G	Ar+H_2	WF_6	ON	Nonselective
H	Ar	WF_6+H_2	ON	Nonselective
I	WF_6+Ar	H_2	ON	Nonselective
J	N_2+H_2	WF_6	ON	Nonselective
K	NH_3+H_2	WF_6	ON	Nonselective
L	NH_3+H_2	WF_6	OFF	Nonselective

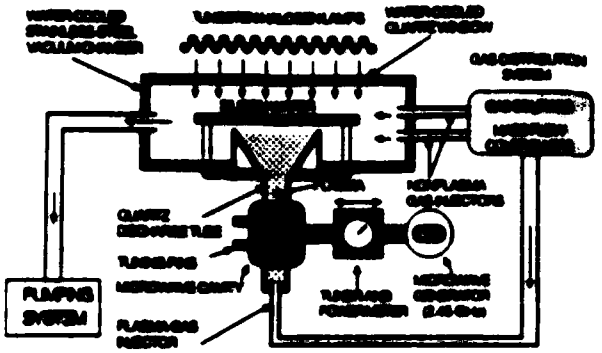

Figure 1. Schematic of the novel cold-wall single-wafer lamp-heated rapid thermal/plasma multiprocessing reactor.

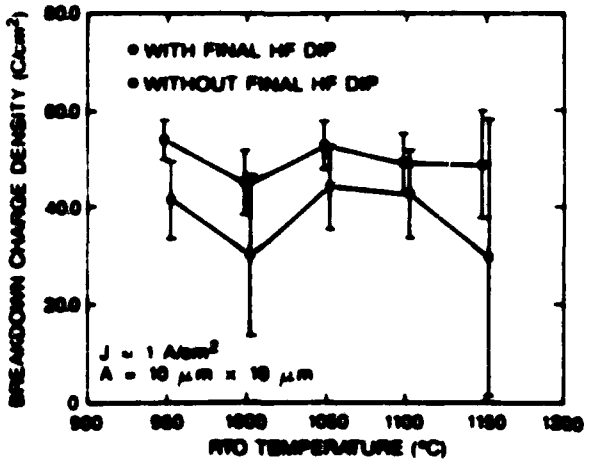

Figure 2. Breakdown charge density vs RTO temperature determined from constant-current TDDB measurements at 1 A/cm² in 10 μm×10 μm unannealed MOS devices (rapidly grown gate oxides) with and without final preoxidation HF dip. No HF dip simulates the surface condition with native oxide such as in the hot-wall furnace oxidations and HF dipped wafers correspond to the in-situ cleaned surfaces prior to oxidation in cold-wall lamp-heated single-wafer reactors.

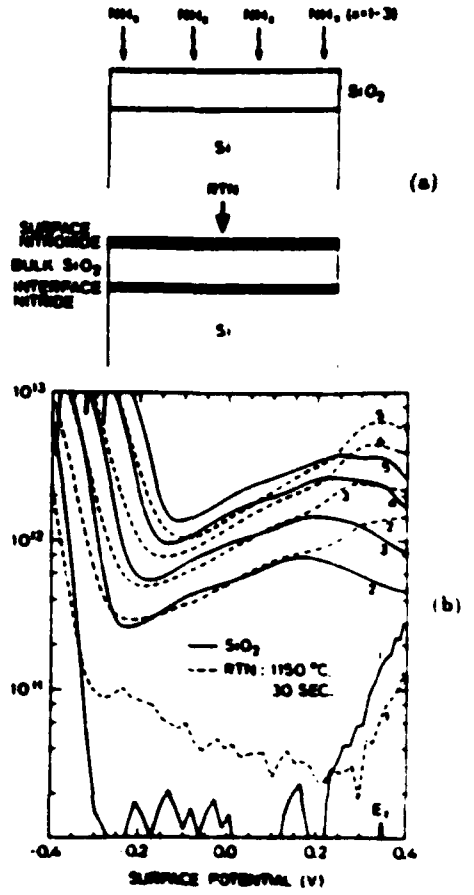

Figure 3. (a) Structural model for nitroxide insulators formed by RTN of SiO_2. (b) Effect of step-by-step high-field constant-current stress on surface-state density in MIS devices (gate area=7.85×10^{-3} cm^2) with 95 Å SiO_2 and nitroxide prepared by RTN at 1150°C for 30 sec.

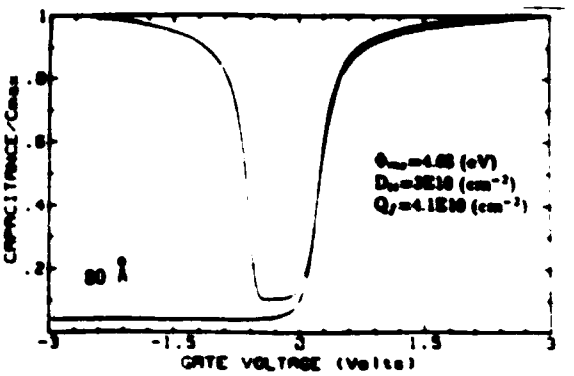

Figure 4. Typical high- and low-frequency C-V characteristics of MOS devices with subhundred angstrom SiO_2 gate insulator and tungsten gate electrode fabricated by formation of amorphous silicon glue layer followed by selective hot-wall LPCVD furnace tungsten deposition.